IN THE SPECIFICATION

Please replace the paragraph beginning at page 1, line 5, with the following paragraph:

This application claims priority to a-n application entitled "Precoder and Optical Duo-Binary Transmission Apparatus Using the Same," filed in the Korean Intellectual Property Office on September 25, 2003 and assigned Serial No. 2003-66587, the contents of which are hereby incorporated herein by reference.

Please replace the paragraph beginning at page 1, line 12, with the following paragraph

The present invention relates to an optical duo-binary transmission apparatus using an optical duo-binary transmission method, and more particularly to a precoder performing [[a]] parallel processing and an optical duo-binary transmission apparatus using the same.

Please replace the paragraph beginning at page 1, line 16, with the following paragraph

A Dense Wavelength Division Multiplexing (hereinafter "DWDM") optical transmission system has excellent communication efficiency, since it can transmit an optical signal having multiple channels with different wavelengths through a single optical fiber. Transmission speed is not a limiting factor, because an optical signal travels at the speed of light through the optical medium. Accordingly, DWDM systems are now widely used in ultra-high speed internet networks, and data traffic on such networks is increasing. ~~Systems in common use employing DWDM technology, as of late, are each capable of transmitting m ore t han a h undred channels t hrough a s ingle o ptical fiber.~~ Systems in common use employing DWDM technology, as of late, are each capable of transmitting more than a hundred channels through a single optical fiber. Furthermore, various research efforts are being actively conducted to develop a system which can transmit more than two hundred 40-gigabits-per-second (Gbps)

channels through a single optical fiber simultaneously, for an overall transmission speed on the order of 10 terabits-per-second (Tbps).

Please replace paragraphs beginning at page 3, line 5, with the following paragraphs

In FIG. 1, the conventional optical duo-binary transmission apparatus includes a multiplexer 10, a precoder 20, a low pass filter 30, a modulator driving amplifier 40, a laser source 50 for outputting a carrier wave, and a Mach-Zehnder interferometer type optical intensity modulator 60. The multiplexer 10 multiplexes data input signals of N number of channels so as to output the multiplexed signal, and the precoder 20 codes the multiplexed signal. The low-pass filter 30 converts a 2-level binary signal outputted from the precoder 20 into a 3-level electrical signal, and reduces the bandwidth of the signal. The modulator driving amplifier 40 amplifies the 3-level electrical signal to output an optical modulator driving signal.

The input signals of N number of channels are multiplexed by the multiplexer 10, and the multiplexed signal is then coded by the precoder 20. The 2-level binary signal outputted from the precoder 20 is inputted to the low-pass filter 30, the low-pass filter having a bandwidth corresponding to about 1/4 of a clock frequency of the 2-level binary signal. This excessive limitation to the bandwidth causes interference between codes, which thus changes the 2-level binary signal to a 3-level duo-binary signal. The 3-level duo-binary signal is amplified by the modulator driving amplifier 40 so as to be used as a driving signal of the Mach-Zehnder interferometer type optical intensity modulator 60. The carrier wave outputted from the laser source 50 is subjected to phase and optical intensity modulation according to the driving signal of the Mach-Zehnder interferometer type optical intensity modulator 60 and is then outputted as a 2-level optical duo-binary signal.

Please replace the paragraphs beginning at page 4, line 19 with the following paragraphs

The present invention has been made to solve the above-mentioned problems occurring in the prior art. A first object of the present invention is to provide a precoder which can achieve a high speed even with existing low-speed electrical elements by coding multiple input data [[inparallel]] in parallel before time division multiplexing. Another object is to provide an optical duo-binary transmission apparatus using the precoder.

In order to accomplish the aforementioned objects, according to one aspect of the present invention, there is provided a precoder that includes a judgment unit for judging whether an odd number or even number of '1's exists in data input signals of N channels inputted at an n^{th} time of channel input. Further included in the precoder is a toggle unit for toggling an output signal of the judgment unit when the number of '1's is judged by the judgment unit to be odd. The toggling determines an output value of one of the N channels. Communicatively connected to the toggle unit is an output unit for determining output values of other channels according to respective ones of the data input signals.

In order to accomplish the aforementioned objects, according to one aspect of the present invention, there is provided an optical duo-binary transmission apparatus that includes a precoder for coding in parallel data input signals of N channels, and a multiplexer for time division multiplexing the signals coded by the precoder.

Please replace the paragraph beginning at page 6, line 8 with the following paragraph

FIG. 7 is a view showing a construction of a precoder performing [[a]] parallel processing according to a first embodiment of the present invention;

Please replace the paragraph beginning at page 6, line 11 with the following paragraph

FIG. 9 is a view showing a construction of a precoder performing [[a]] parallel processing according to a second embodiment of the present invention; and

Please replace the paragraph beginning at page 7, line 14 with the following paragraph

When input signals are a_{4n+1}, a_{4n+2}, a_{4n+3}, and a_{4n+4}, a signal 'b_{4n+1}' can be obtained by XORing the signal 'a_{4n+1}' and a signal, which is achieved by time-delaying the signal 'b_{4n+4}' by 1 data bit. A signal 'b_{4n+2}' can be obtained by XORing the signal 'b_{4n+1}' and the signal 'a_{4n+2}'. Signals 'b_{4n+3}' and 'b_{4n+4}' can be obtained in the same manner as described above. That is, the following-[[logic al]] logical operations are performed.

Please replace the paragraph beginning at page 7, line 20, with the following paragraph:

In FIG. 7, a d-flipflop (D-FF) ~~c an b e u sed for delaying t ime b y 1 d ata b it, a nd~~ can be used for delaying time by 1 data bit, and another XOR gate can be inserted into a path in which an XOR gate is not used for compensating for time delay at the XOR gate. In this case, the time delay can be compensated for without variation of the signal by inputting a "0" level signal to one input of the XOR gate.

Please replace the paragraph beginning at page 8, line 5, with the following paragraph:

FIG. 8 is a view showing input/output signals in FIG. 7 when an input signal is '1101011110010100'. In FIG. 8, if the input signals In1 to In4 are time-multiplexed, ~~the multiplexed s ignal i s e qual t o t he i nput s ignal I n F IG. 4~~ the multiplexed signal is equal to the input signal in FIG. 4. ~~If t he s ignals O ut1 a nd O ut4~~ If the signals Out1 and Out4 obtained through the parallel processing are respectively time-multiplexed, the multiplexed signals are

equal to the output signal in FIG. 4. That is, coding is performed in the same manner as that of the prior art (see FIG. 7).

Please replace the paragraph beginning at page 8, line 11, with the following paragraph:

The precoder 700 according to the first embodiment can be easily realized. However, as the number [['n']]-'N' of the input signals increases, the time delay occurring at the XOR gate is accumulated. Therefore, time delay longer than 1 data bit may occur. Accordingly, the first embodiment is more effective when the number of the input signals is small.

Please replace the paragraph beginning at page 8, line 20, with the following paragraph:

FIG. 9 is a view showing an exemplary construction of a precoder 900 performing [[a]] parallel processing according to a second embodiment of the present invention, and FIG. 10 is a view showing an example of the input/output signals in FIG. 9.

Please replace the paragraph beginning at page 9, line 1, with the following paragraph:

According to the second embodiment, a feed-forward method is used, so that the number ~~o f i nput s ignals i s n ot l imited~~ of input signals is not limited. ~~For s implicity o f d emonstration, a n e xample i n~~ For simplicity of demonstration, an example in which the number N of input signals is 4 will be described below.

Please replace the paragraph beginning at page 9, line 6 with the following paragraph

Referring to FIGs. 9 and 10, the judgment unit 910 judges whether an odd number or even number of '0's exists in N number of input signals inputted at an n^{th} time of signal input. For instance, in the case in which the number N of the input signals is even, the judgment unit

910 outputs '0' when the total number of '1's in the N number of input signals is even. On the other hand, the judgment unit 910 outputs '1' when the total number of '1's in the N number of input signals is odd. FIG. 10 shows an example of the signals as described above. The judgment unit 910 has a construction in which XOR gates are mutually connected in a pyramid configuration. If the number of the input signals increases, the number of the XOR gates also increases. When the number N of the input signals is 4, the judgment unit 910 includes three XOR gates, herein labeled XOR1, XOR2, and XOR3.

Please replace the paragraph beginning at page 9, line 17, with the following paragraph:

When an output signal of the judgment unit 910 is '1' (i.e. when the number of '1's in the input signals is odd), the toggle unit 920 toggles an output signal of the judgment unit 910. The toggle unit 920 includes an AND gate AND1 and a toggle flip-flop (hereinafter, referred to as a T-FF) and ANDs the output signal of the judgment unit 910 and the clock signal CLK. Further, the toggle unit 920 enables the ANDed signal to pass through the T-FF, while generating the n^{th} output signal b_{4n+4} (i.e. Out4). Then, the signal obtained by ANDing the output signal of the judgment unit 910 and the clock signal CLK is inputted to the T-FF, and a toggle of the ~~inputted~~ signal output by the AND gate occurs at each rising edge (marked by an arrow in FIG. 10) of the ~~inputted signal~~ AND output.